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INS_i	effect on i	effect on RAM	effect on ST	effect on s
inc	$i \leftarrow (i+1)$	none	$ST[s] \leftarrow (ST[s]+1)$	none
dec	$i \leftarrow (i+1)$	none	$ST[s] \leftarrow (ST[s]-1)$	none
pop	$i \leftarrow (i+1)$	none	$ST[s] \leftarrow \text{undef}$	$s \leftarrow (s-1)$
push0	$i \leftarrow (i+1)$	none	$ST[s+1] \leftarrow (0)$	$s \leftarrow (s+1)$
load x	$i \leftarrow (i+1)$	none	$ST[s+1] \leftarrow \text{RAM}[x]$	$s \leftarrow (s+1)$
load IO	$i \leftarrow (i+1)$	none	$ST[s+1] \leftarrow \text{IO}$	$s \leftarrow (s+1)$
load RNG	$i \leftarrow (i+1)$	none	$ST[s+1] \leftarrow \text{RNG}$	$s \leftarrow (s+1)$
store x	$i \leftarrow (i+1)$	$\text{RAM}[x] \leftarrow ST[s]$	$ST[s] \leftarrow \text{undef}$	$s \leftarrow (s-1)$
store IO	$i \leftarrow (i+1)$	$\text{IO} \leftarrow ST[s]$	$ST[s] \leftarrow \text{undef}$	$s \leftarrow (s-1)$
if L	if $ST[s]=0$ then $i \leftarrow (i+1)$ if $ST[s] \neq 0$ then $i \leftarrow L$	none	$ST[s] \leftarrow \text{undef}$	$s \leftarrow (s-1)$
goto L	$i \leftarrow L$	none	none	none
xor	$i \leftarrow (i+1)$	none	$ST[s-1] \leftarrow (ST[s-1] \oplus ST[s])$ $ST[s] \leftarrow \text{undef}$	$s \leftarrow (s-1)$
mul	$i \leftarrow (i+1)$	none	def $\alpha = ST[s-1] \times ST[s]$ $ST[s-1] \leftarrow \alpha \bmod 256$ $ST[s] \leftarrow \alpha \text{ div } 256$	none
div	If $ST[s]=0$ then $i \leftarrow \text{AdExcDiv}$ if $ST[s] \neq 0$ then $i \leftarrow (i+1)$	none	If $(ST[s-1] \neq 0)$ do $ST[s] \leftarrow ST[s]/ST[s-1]$	none
		effect on NVM		
getstatic x	$i \leftarrow (i+1)$	none	$ST[s+1] \leftarrow \text{NVM}[x]$	$s \leftarrow (s+1)$
putstatic x	$i \leftarrow (i+1)$	$\text{NVM}[x] \leftarrow ST[s]$	$ST[s] \leftarrow \text{undef}$	$s \leftarrow (s-1)$

FIGURE 1

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0. The X μ P initializes $i \leftarrow 1$
1. The X μ P requests the instruction number i from the XT
2. The XT sends the INS_i to the X μ P
3. The X μ P executes INS_i
4. Go to step 1.

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FIGURE 2

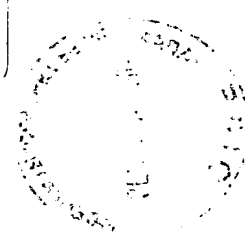
INS_i	Alert = TRUE if
If L	$\phi(ST[s]) = 1$
div	$\phi(ST[s]) = 1$
store IO	$\phi(ST[s]) = 1$
putstatic x	$\phi(NVM[x]) = 1$

FIGURE 3

INS_i	Alert = TRUE if
If L	$\phi(ST[s]) = 1$
Div	$\phi(ST[s]) = 1$
Store IO	$\phi(ST[s]) = 1$
putstatic x	Always

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FIGURE 4



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INS _i	Effect on Φ
Inc	None
dec	None
pop	$\phi(ST[s]) \leftarrow 0$
push0	$\phi(ST[s+1]) \leftarrow 0$
load x	$\phi(ST[s+1]) \leftarrow \phi(RAM[x])$
load RNG	$\phi(ST[s+1]) \leftarrow 1$
store x	$\phi(RAM[x]) \leftarrow \phi(ST[s])$ $\phi(ST[s]) \leftarrow 0$
load IO	$\phi(ST[s+1]) \leftarrow 0$
store IO	$\phi(ST[s]) \leftarrow 0$
if L	$\phi(ST[s]) \leftarrow 0$
goto L	None
Xor	$\phi(ST[s-1]) \leftarrow \phi(ST[s-1]) \vee \phi(ST[s])$ $\phi(ST[s]) \leftarrow 0$
mul	$\phi(ST[s]), \phi(ST[s-1]) \leftarrow \phi(ST[s-1]) \vee \phi(ST[s])$
div	$\phi(ST[s]), \phi(ST[s-1]) \leftarrow \phi(ST[s-1]) \vee \phi(ST[s])$
getstatic x	$\phi(ST[s+1]) \leftarrow \phi(NVM[x])$
putstatic x	$\phi(NVM[x]) \leftarrow \phi(ST[x])$ $\phi(ST[s]) \leftarrow 0$

FIGURE 5